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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/746,328	12/20/2000	William G. Hooper III	10001025-1	1710

7590 08/10/2004

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EXAMINER	
PATEL, HETUL B	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 08/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/746,328	HOOPER, WILLIAM G.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,15 and 17* is/are rejected.

7)☒ Claim(s) *14,16 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. This action is responsive to communication filed on June 17, 2004. This amendment has been entered and carefully considered. Claims 1-18 are again presented for examination.

2. Applicant's arguments filed on June 17, 2004 have been fully considered but they are not persuasive.

3. The rejection of claims 1-13, 15 and 17 as in the Office Action mailed February 11, 2004 is respectfully maintained and reiterated below for Applicant's convenience.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2, 4-5, and 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dobbek (USPN: 6,535,995) in view of Bruce et al. (USPN: 6,000,006) hereinafter, Bruce.

As per claim 1, Dobbek teaches a direct access storage device (DASD) which converts logical address to physical address and replaces the defective sector of

memory with the fresh unused defect-free sector (e.g. see abstract). This storage device comprising:

- a physical memory including a spare table region containing spare tables (e.g. see column 4, lines 23-36 and figure 3)
- an memory interface that provides, to devices that access the memory, memory operations directed to target data blocks specified by the accessing device via a logical data block address (e.g. see column 2, lines 29-32 and figure 2)
- a logic component that maps a logical data block address to a physical address describing the location of a data block in the memory (e.g. see column 4, lines 8-16 and lines 23-36).

Further limitation of having a data page region and a spare page region in the DASD is embedded in the prior art taught by Dobbek. Dobbek teaches that there are a predetermine number of data sectors and spare locations available in each virtual sector (e.g. see lines 43-48, column 4). Here, the data page region is created using the data sectors to store the data and the spare page region is created using the spare locations in order to store the data for replacing defected region data. However, Dobbek does not teach that this data block sparing technique that applied over the direct access storage device can also be applied to the solid-state storage device. Bruce, on the other hand, teaches that a flash memory system provides solid-state mass storage as a replacement to a DASD (a hard disk) (e.g. see abstract). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of

the current invention was made to use the solid-state storage device in the place of the DASD as taught by Bruce in the Dobbek's storage device because (1) the solid-state storage device has a very high storage density, i.e. the physical size of the solid-state storage device is less than the DASD to store the same amount of data and (2) the solid-state storage device is a lot faster and have a longer life compare to the DASD.

As per claim 2, Dobbek and Bruce disclose the claimed invention as described above and furthermore, Dobbek teaches that the file logical block address (FLBA) contains virtual track number, which indexes the correct track in the virtual track (VT) table and it's also used as an index in the virtual sector (VS) table (e.g. see column 5, lines 36-38). Here, the virtual track number acts as both page index and the data block index.

As per claims 4-5, Dobbek and Bruce disclose the claimed invention as described above and furthermore, the combination of Dobbek and Bruce teaches a solid-state data storage device, which includes spare table region, spare page region and data page region as explained in the rejection of claim 1 above. It is very well known in the art that any storage device can be partitioned into multiple different regions with different sizes. Here the inventor is partitioning the solid-state storage device into five different regions and starting from lower addressed portion to higher addressed portion of the storage device, calling those regions as a first spare table region, a first spare page region, a data page region, a second spare page region and a second spare table region, respectively.

As per claims 9 and 11, Dobbek and Bruce disclose the claimed invention as described above and furthermore, the combination of Dobbek and Bruce teaches a solid-state data storage device. The memory size is a system dependent feature. Since neither applicant nor specification disclose changing the size of the memory (i.e. data page, spare page and spare table element) would change the system functionality or performance, therefore, any size of the memory can be selected, by this rationale, claims 9 and 11 are rejected.

As per claim 10, the combination of Dobbek and Bruce teaches a DASD, which includes spare table region, spare page region and data page region as explained in the rejection of claim 1 above. It is very well known in the art that any storage device can be partitioned into multiple different regions with different sizes in such a way so

- a spare table contains a number of elements equal to the number of data blocks within data page,
- a spare table region contains a number of spare tables equal to the number of data pages within data page region, and
- a spare page region contains a number of spare pages equal to the number of data pages within data page region,

to keep the redundant copies of the data stored in data blocks and data pages for the backup purpose so the spare data will be available for replacing the defected data in the data page region. Unlike the further limitation, the spare block map can be stored in any spare data block of the spare page. But by storing it in the first spare data block of the spare page, the access time to access the status information, which stored in the

spare data block, can be reduced. And the overall performance of the storage device can be increased since this status information get read every time the spare data block get called and every time the access time to read that will be lowered.

As per claim 12, Dobbek and Bruce disclose the claimed invention as described above and furthermore, Dobbek teaches a method for converting logical address to physical address in a DASD, comprising:

- providing memory including a spare table region containing spare tables (e.g. see column 4, lines 23-36 and figure 3);
- extracting a page index and a data block index from the logical data block address, and uses the page index to locate a corresponding spare table and the data block index to locate a corresponding spare table element within the corresponding spare table (e.g. see column 5, lines 36-38). Here, as explained above in the rejection of the claim 2, the virtual track number acts as both page index and the data block index. First, the virtual track number indexes the correct track in the virtual track (VT) table, just like the page index gets used to locate the correct spare table in this application and then the virtual track number also used as an index in the virtual sector (VS) table, just like the data block index gets used to locate the correct spare table element in this application.

However, Dobbek does not teach that this method for converting logical address to physical address, which applied over DASD, can be applied to the solid-state storage device. Bruce, on the other hand, teaches that a flash memory system provides solid-

state mass storage as a replacement to a DASD (a hard disk) (e.g. see abstract). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to use the solid-state storage device in the place of the DASD as taught by Bruce in the Dobbek's storage device because (1) the solid-state storage device has a very high storage density, i.e. the physical size of the solid-state storage device is less than the DASD to store the same amount of data and (2) the solid-state storage device is a lot faster and have a longer life compare to the DASD.

5. Claim 3, 13 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dobbek in view of Bruce as applied to claim 1-2, 4-5, and 9-12 above, further in view of Jeddeloh (USPN: 5,933,852).

As per claim 3, the combination of Dobbek and Bruce teaches the invention as claimed including the logic component which extracts page index and data block index from the logical data block address, and uses the page index to locate a corresponding spare table and the data block index to locate a corresponding spare table element within the corresponding spare table (e.g. see column 5, lines 36-38). Here, as explained above in the rejection of the claim 2, the virtual track number acts as both page index and the data block index. First, the virtual track number indexes the correct track in the virtual track (VT) table, just like the page index gets used to locate the correct spare table in this application and then the virtual track number also used as an index in the virtual sector (VS) table, just like the data block index gets used to locate the correct spare table element in this application. However, Dobbek and Bruce do not particularly disclose that when a status indication indicates that the logical block

address has been remapped, the data storage device uses page offset and page index to determine the physical address of the data block within the spare page and the data storage device uses page index and data block index to determine the physical address of the data block within the data page if the status indication indicates that the logical block address has not been remapped.

Jeddeloh, on other hand, in his teaching of system and method for accelerated remapping of defective memory locations, disclose that "the non-defective memory portion to which the requested memory portion is mapped in either the usage table or the remapping table is accessed if the requested memory portion is defective, and the requested memory portion is accessed if the requested memory portion is not defective" (e.g. see the abstract). Here, the usage table and the remapping table contain the addresses, which are already offset so it can represent the appropriate spare location. Accordingly, it would be obvious to one of ordinary skill in the art at the time of current invention was made to add the defective address remapping circuit/module, which provides a spare location address if the requested address is defective as taught by Jeddeloh. In doing so, it would prevent the data from getting corrupted by not reading and writing on a defective memory location.

As per claim 13, see arguments with respect to the rejection of claims 1-3.

As per claim 17, see arguments with respect to the rejection of claim 3.

6. Claim 6 rejected under 35 U.S.C. 103(a) as being unpatentable over Dobbek in view of Bruce further in view of Venkatesh et al. (USPN: 6,397,292), hereinafter, Venkatesh.

As per claim 6, the combination of Dobbek and Bruce teaches the solid-state storage device as claimed. However, neither Dobbek nor Bruce particularly disclose that redundant copies of the spare tables of the first spare table region are stored in the second spare table region. Venkatesh, on the other hand, teaches that redundant data storage is a common technique for providing a desired degree of reliability and availability of data storage access (e.g. see lines 22-34, column 1). Here, Venkatesh makes redundant copies of whole disk drives as a backup copies in case of data loss/corruption occurs in the original disk drive(s). Using the same concept, it would be obvious to one of ordinary skill in the art at the time of current invention was made to keep redundant copies of the spare tables of the first spare table region into the second spare table region, as taught by Venkatesh, in order to continue spare table element access operations in the event of a failure of first spare table region.

7. Claims 7-8 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dobbek in view of Bruce further in view of Smith (USPN: 6,269,432).

As per claims 7-8, the combination of Dobbek and Bruce teaches the solid-state storage device as claimed. However, neither Dobbek nor Bruce particularly disclose that the solid-state storage device comprises a spare table cache and a cached spare table identifier register and they get used in order to map the logical data block address to a physical address. Smith, on other hand, teaches that the cache memory get used to increase the processing speed of the system and a register get used to point to a location in the cache where previously stored data resides (see lines 12-20, column 1).

Accordingly, it would be obvious to one of ordinary skill in the art at the time of current invention was made to modify the storage device of Dobbek and Bruce by adding a spare table cache and a cached spare table identifier register as taught by Smith to decrease the time to convert the logical data block address to physical address. In doing so, the mapping process to map the logical data block address to a physical address gets faster because spare table elements and spare blocks get read from the cached spare table identifier register and the spare table cache, respectively, which are a lot faster than reading them from the spare tables and the spare pages, respectively.

As per claims 15, see arguments with respect to the rejection of claim 8.

Allowable Subject Matter

8. Claims 14, 16 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Remarks

9. As to the remark, Applicant asserted that "he cannot find a suggestion in the prior art, the cited references, or in any statement or justification offered by the Examiner, for using Bruce's flash-memory in place of a hard-disk, only after altering Bruce's device to use a hard-disk-like bad-block replacement mechanism, rather than Bruce's claimed block remapping scheme. " (page 5, paragraph 2).

Examiner respectfully traverses Applicant's remark for the following reasons:

10. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

11. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). "There are three possible sources for a motivation to combine references: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art." In re Rouffet, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998).

In this case, Dobbek teaches the data block sparing technique as claimed by the applicant that applied over the direct access storage device. However, Dobbek does not teach that this data block sparing technique that applied over the direct access

storage device can also be applied to the solid-state storage device. Bruce, on the other hand, teaches that a flash memory system provides solid-state mass storage as a replacement to a DASD (a hard disk) (e.g. see abstract). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to use the solid-state storage device in the place of the DASD as taught by Bruce in the Dobbek's storage device because (1) the solid-state storage device has a very high storage density, i.e. the physical size of the solid-state storage device is less than the DASD to store the same amount of data and (2) the solid-state storage device is a lot faster and have a longer life compare to the DASD.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is (703) 305-6219. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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